CLAIMS

What is claimed is:

1. A semiconductor device comprising a field effect transistor formed on a SOI substrate, the semiconductor device characterized in comprising:

a gate region formed on a semiconductor film of the SOI substrate;

source and drain regions each spaced a specified distance from a channel region formed in the semiconductor film below the gate region;

a first extension region that extends from the source region to the channel region; and

a second extension region that extends from the drain region to the channel region,

wherein junction depths of the first and second extension regions are formed to be shallower than junction depths of the source region and the drain region.

2. A semiconductor device according to claim 1, wherein the junction depth of each of the first and second extension regions is 50% or less of the junction depth of each of the source region and the drain region.

3. A semiconductor device according to claim 1 or claim 2 characterized in operating in a fully depleted operation mode.

4. A semiconductor device according to any one of claim 1 through claim 3, wherein the SOI substrate is a substrate composed of a glass substrate, a quartz substrate or another insulation substrate and a semiconductor film formed thereon.

5. A method for manufacturing a semiconductor device, comprising a method for manufacturing a field effect transistor to be formed on a SOI substrate, the method characterized in comprising:

a first step of forming a gate electrode on a semiconductor layer of the SOI substrate;

a second step of implanting an impurity with a high concentration in regions spaced specified distances from the gate electrode to form source and drain regions;

a third step of introducing an impurity in regions between a channel region formed under the gate electrode and the source and drain regions to a depth shallower than the source and drain to form extension regions of the source and drain regions; and

a fourth step of electrically activating the extension regions by a laser anneal method.

6. A method for manufacturing a semiconductor device according to claim 5, wherein the third step includes extremely shallowly implanting an impurity by a plasma doping method.

7. A method for manufacturing a semiconductor device according to claim 6, wherein the third step includes activating the impurity by a laser anneal method.

SUB 42) 8. A method for manufacturing a semiconductor device according any one of claim 5 through claim 7, wherein the junction depth of the extension regions is formed to be 50% or less of the junction depth of each of the source region and the drain region.